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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known	
Application Number	10/674,085
Filing Date	September 29, 2003
First Named Inventor	Elias Fallon et al.
Group Art Unit	~~Not Yet Assigned~~ 2825
Examiner Name	~~Not Yet Assigned~~ Helen Rossoshek
Attorney Docket Number	2879-030564

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2]	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
HR	1	6,161,078		Ganley	12/12/2000	———
HR	2	6,282,694		Cheng et al.	08/28/2001	———
HR	3	6,550,046	B1	Balasa et al.	04/15/2003	———

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, cite and/or country where published.	T[2]
HR	4	FLORIN BALASA and KOEN LAMPAERT, "Module Placement For Analog Layout Using The Sequence-Pair Representation", Proc. ACM/IEEE Design Automation, pp. 274-279, (June 1999).	
↓	5	FLORIN BALASA and KOEN LAMPAERT, "Symmetry Within The Sequence-Pair Representation In The Context Of Placement For Analog Design", IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 19, No. 7, pp. 721-731 (July 2000).	
↓	6	FLORIN BALASA, "Device-Level Placement For Analog Layout: An Opportunity For Non-Slicing Topological Representations", Proc. Asia-Pacific DAC (ASPDAC), pp. 281-286, (2001).	
↓	7	ERIC FELT, ENRICO MALAVASI, EDOARDO CHARBON, ROBERTO TOTARO and ALBERTO SANGIOVANNI-VINCENTELLI, "Performance-Driven Compaction For Analog Integrated Circuits", IEEE 1993 Custom Integrated Circuits Conference, pp. 17.3.1-17.3.5, (1993).	
↓	8	Eric FELT, EDOARDO CHARBON, ENRICO MALAVASI and ALBERTO SANGIOVANNI-VINCENTELLI, "An Efficient Methodology For Symbolic Compaction Of Analog IC's With Multiple Symmetry Constraints", Proc. European Design Automation Conference, pp. 148-153, (1992).	
↓	9	JOSEPH L. GANLEY, "Efficient Solution Of Systems Of Orientation Constraints", In Proceedings Of The International Symposium On Physical Design, pp. 140-144, (1999).	
↓	10	PEI-NING GUO, CHUNG-KUAN CHENG and TAKESHI YOSHIMURA, "An O-Tree Representation Of Non-Slicing Floorplan And Its Applications", Proc. ACM/IEEE Design Automation Conference, pp. 268-273, (June 1999).	
↓	11	EN-CHENG LIU, MING-SHIUN LIN, JIANBANG LAI and TING-CHI WANG, "Slicing Floorplan Design With Boundary-Constrained Modules", ISPD'01, pp. 124-129, April 1-4 (2001).	
↓	12	ENRICO MALAVASI, JOSEPH L. GANLEY and EDOARDO CHARBON, "Quick Placement With Geometric Constraints", IEEE 1997 Custom Integrated Circuits Conference, pp. 561-564, (May 1997).	
HR	13	C. BRANDOLESE, M. PILLAN, F. SALICE and D. SCIUTO, "Analog Circuits Placement: A Constraint Driven Methodology", IEEE, pp. 635-638, (1996).	

Examiner Signature	/Helen Rossoshek/	Date Considered	05/04/2006

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

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HR	14	MARGHERITA PILLAN and DONATELLA SCIUTO, "Constraint Generation And Placement For Automatic Layout Design Of Analog Integrated Circuits", pp. 355-358.	
↓	15	YINGXIN PANG, FLORIN BALASA, KOEN LAMPAERT and CHUNG-KUAN CHENG, "Block Placement Symmetry Constraints Based On The O-Tree Non-Slicing Representation", Proc. ACM/IEEE Design Automation Conference, pp. 464-467, (June 2000).	
	16	JUAN A. PRIETO, JOSE M. QUINTANA, ADORACION RUEDA and JOSE L. HUERTAS, "An Algorithm For The Place-And-Route Problem In The Layout Of Analog Circuits", Pro. IEEE ISCAS, pp. 491-494 (1994).	
	17	D. F. WONG and C. L. LIU, "A New Algorithm For Floorplan Design", Proceedings Of The 23rd ACM/IEEE Design Automation Conference, pp. 101-107, (July 1986).	
	18	JOHN M. COHN, DAVID J. GARROD, ROB A. RUTENBAR and L. RICHARD CARLEY, "KOAN/ANAGRAM II: New Tools For Device-Level Analog Placement And Routing," IEEE Journal Of Solid-State Circuits, Vol. 26, No. 3, pp. 330-342, (March 1991).	
	19	D. W. JEPSEN and C.D. GELLAT JR., "Macro Placement By Monte Carlo Annealing", Proc. IEEE International Conference On Computer Design, pp. 495-498, (November 1984).	
	20	ENRICO MALAVASI, EDOARDO CHARBON, GANI JUSUF, ROBERTO TOTARO and ALBERTO SANGIOVANNI-VINCENTELLI, "Virtual Symmetry Axes For The Layout Of Analog IC's", Proc. 2nd ICVC, pp. 1-10, (October 1991).	
	21	JURGEN M. KLEINHANS, GEORG SIGL, FRANK M. JOHANNES and KURT J. ANTREICH, "GORDIAN: VLSI Placement By Quadratic Programming And Slicing Optimization", IEEE Transactions On Computer-Aided Design, Vol. 10, No. 3, pp. 356-365, (March 1991).	
↓	22	HIROSHI MURATA, KUNIHIRO FUJIYOSHI, SHIGETOSHI NAKATAKE and YOJI KAJITANI, "VLSI Module Placement Based On Rectangle-Packing By The Sequence-Pair", IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 15, No. 12, pp. 1518-1524, (December 1996).	
HR	23	SUJOY MITRA, SUDIP K. NAG, ROB A. RUTENBAR and L. RICHARD CARLEY, "System-Level Routing Of Mixed-Signal ASICS In WREN", Proc. ACM/IEEE International Conference On CAD, pp. 394-399, (November 1992).	

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Sheet	3	of	3

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HR	24	R. OKUDA, T. SATO, H. ONODERA and K. TAMARU, "An Efficient Algorithm For Layout Compaction Problem With Symmetry Constraints", In Proc. IBBB ICCAD, pp. 148-151, (November 1989).	

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